TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
YUSO-131

In Re Application Of: **Hsieh et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/052,989	11/9/2001	David Vu		2818	1309

Invention: **Formation of electroplate solder on an organic circuit board for flip chip joints and board to board solder joints**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 29, 2005**

The fee for filing this Appeal Brief is: **$500.00**

☒ A check in the amount of the fee is enclosed.

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Dated: 5-25-05

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. YUSO-131

In re patent application of

Hsieh et al.

Group Art Unit: 2818

Serial No. 10/052,989

Examiner: David Vu

Filed: November 9, 2001

For: Formation of Electroplate Solder on an Organic Circuit Board for Flip Chip Joints and Board to Board Solder Joints

APPEAL BRIEF UNDER 37 C.F.R. § 1.192

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Commissioner for Patents
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Dear Sir:

This appeal is taken from the final rejection dated December 29, 2004, in which claims 24-33, 44 and 45 were finally rejected. This appeal brief is being filed in triplicate together with a check in the amount of $500.00.

1. Real Party in Interest - 37 C.F.R. § 1.192(c)(1)

The real party in interest is the Appellant, Phoenix Precision Technology Corp., of Taiwan.

2. Related Appeals and Interferences – 37 C.F.R. § 1.192(c)(2)

There are no related appeals and interferences.

3. Status of Claims - 37 C.F.R. § 1.192(c)(3)

Claims 24-27, 32-33 and 44 stand rejected under 35 U.S.C. § 102(e) as being anticipated by USP 6,375,062 to Higdon et al. (hereinafter "Higdon").

Claims 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Higdon in view of USP 6,387,734 to Inaba et al. (hereinafter "Inaba").

Claims 30-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Higdon in view of Inaba as applied to claims 24 and 29 above, and further in view of USP 3,958,048 to Donovan et al. (hereinafter "Donovan").

Claim 45 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Higdon in view of USP 5,822,856 to Bhatt et al. (hereinafter "Bhatt").

No claim has been allowed.

Appellant appeals the rejections of claims 24-33, 44 and 45. A copy of these claims is appended hereto.

4. Status of Amendment(s) - 37 C.F.R. § 1.192(c)(4)

No amendments have been filed after the final rejection. Thus, all amendments which have been filed have been entered.

A notice of appeal is being timely filed, concurrently with this brief.

5. Summary of the Invention - 37 C.F.R. § 1.192(c)(5)

The claimed invention relates, generally, to electronic packages, and in particular, to flip chip joints and board-to-board solder joints formed by electroplated solder on ***organic circuit boards***. The present invention aims to provide a method of forming a metal seed layer on an organic circuit board without damaging the solder mask layer.

Referring to FIGS. 3A-3G, the claimed invention is directed to a method of forming electroplated solder on an organic circuit board for making flip chip joints and board to board solder joints. First, the invention provides an organic circuit board 305 having a surface bearing electrical circuitry that includes at least a contact pad 310. A solder mask layer 320 is formed on the surface, with the solder mask being patterned to expose the contact pad. See FIG. 3A and page 6, lines 1-16 of the specification. Next, a thin metal seed layer 325 is formed over the surface, with the

seed layer being solely made of a first metal material. See FIG. 3B and page 6, line 17 to page 7, line 21, and page 7, line 28 to page 8, line 35 of the specification. A resist layer 330 is then formed with at least one opening 335 located at the contact pad 310 that is deposited over the seed layer 325. Then, a solder bump 340 is formed in the opening 335 by electroplating, with the solder bump 340 containing at least the first metal material. See FIG. 3C and page 7, lines 21-24 of the specification. The resist layer 330 and the seed layer 325 (beneath the resist layer 330) are then removed. See FIG. 3D and page 7, lines 24-25 of the specification. The seed layer 325 beneath the solder bump 340 dissolves completely into the solder bump after a reflow process, and disappears. See FIG. 3F and page 8, lines 8-11 of the specification.

6. Issues On Appeal - 37 C.F.R. § 1.192(c)(6)

(A) Whether claims 24-27, 32-33 and 44 are anticipated within the meaning of 35 U.S.C. § 102(e) by Higdon.

(B) Whether obviousness of claim 45 is established within the meaning of 35 U.S.C. § 103(a) based on the combined teachings of Higdon and Bhatt.

7. Grouping of Claims - 37 C.F.R. § 1.192(c)(7)

Claims 24-33 belong to the first group of claims, and claims 44-45 belong to the second group of claims.

There is one independent claim on appeal, claim 24.

8. Appellant's Argument - 37 C.F.R. § 1.192(c)(8)

A. Claims 24-27 and 32-33 are patentably distinguished over Higdon within the meaning of 35 U.S.C. §102(e).

In the Final Office Action dated December 29, 2004, claims 24-27 and 32-33 were rejected under 35 U.S.C. 102(e) as being anticipated by Higdon. As shown below, this rejection is improper and should be reversed and withdrawn.

Claim 24 is the only independent claim, and recites a method of forming electroplated solder on an ***organic circuit board*** for making flip chip joints and

board to board solder joints. The claimed method includes the step of providing an organic circuit board 305 having a surface bearing electrical circuitry that includes at least a contact pad 310. The claimed method then recites steps (see "Summary of the Invention" section above) for forming a solder bump 340 where the seed layer 325 beneath the solder bump 340 dissolves completely into the solder bump after a reflow process, and disappears.

Higdon does not teach or suggest the application of the claimed steps on an organic circuit board, but instead discloses a surface bumping method for use on a conventional IC chip. Thus, Higdon does not disclose the claimed step of "providing an organic circuit board".

The Examiner relies on column 1, lines 23-25 of Higdon as disclosing an organic circuit board. This language is in the "Background" section of Higdon, and was referring to surface-mount (SM) semiconductor devices such as flip chips. Higdon states that these flip chips have a circuit board that "...may be a ceramic substrate, printed wiring board, flexible circuit or silicon substrate, though other substrates are possible." Applicant argued that this language does not include an organic circuit board, and the Examiner responded by arguing that:

> "Higdon discloses the circuit board may be a flexible circuit (col. 1, lines 23-25). The terminology 'flexible circuit' is a recognized term of art when referring to an organic substrate (Please refer to US Patent 6,392,143, col. 6, lines 14-18)." Page 6 of Final Office Action dated 12/29/04.

In response, Applicant respectfully submits that this reference in column 1, lines 23-25 of Higdon to a "flexible circuit" was taken in the context of discussing the prior art. In addition, column 1, lines 18-23 of Higdon state that:

> "[t]he terminals are typically in the form of solder bumps near the edges of the chip, and serve to both secure the chip to a circuit board and electrically interconnect the flip chip circuitry to a conductor pattern on the circuit board."

This language only discloses the formation of solder bumps on an IC chip, and serve to both secure the chip to a circuit board and electrically interconnect the flip chip circuitry to a conductor pattern on the circuit board.

In fact, Higdon discloses his method (in the Detailed Description section) for forming solder bumps by electroplating, and only discloses the fabrication of solder bumps on an IC chip, which is not the same technology as the solder bump 340 formed on an organic circuit board 305 that is claimed in the present invention.

A person skilled in the relevant art would know that the steps taught by Higdon in its "Detailed Description" section cannot be applied to a conventional organic circuit board because there are significant differences between an organic circuit board and a conventional IC chip which make it impossible to apply the technology and methods for IC chips onto organic circuit boards.

The present invention is directed to "organic" circuit boards. Organic circuit boards are well-known in the art, and examples of the materials used for these organic circuit boards are set forth on page 6, lines 1-7 of the specification. These materials clearly distinguish the nature of the circuit board (or substrate), and are recited in dependent claims 44-45 to further distinguish the silicon substrate of Higdon (see next section below).

Applicant respectfully submits that there are significant differences between the processes for forming the electroplated solders on an IC chip and an organic substrate. It is impossible to employ the techniques and processes of an IC chip directly to an organic substrate. First, it is noted that the passivation layer formed on the IC chip (such as disclosed in Higdon) is made of silicon oxide or silicon nitride, which are capable of being exposed to high temperature and acid/alkali environments. However, solder masks used on an organic substrate are made of light-sensitive epoxy resin or acrylic resin, which cannot tolerate high temperature or high acid/alkali environments. Thus, application of the high temperatures and acid/alkali environments used for the IC chip will destroy the organic substrate.

In addition, the semiconductor processes, chemical solutions and conditions of manufacturing used for IC chips are very different from the manufacturing processes, conditions and chemical solutions of the electroplated solders for the

organic substrate. For example, the chemical solutions used for IC chips would attack the organic substrate.

In this regard, Applicant is enclosing herewith copies of relevant pages (cover sheet, abstract and pages 10-19) of a publication entitled "UBM Formation on Single Die/Dice for Flip Chip Applications", Suwanna Jittinorasett, August 25, 1999. The disclosures in this publication support the position taken by Applicant.

First, page 14 of this publication discloses that the photo resister residues on the opening are removed by plasma etching before electroplating. The passivation layer can be a polyimide, which is a very stable material, so plasma etching on the passivation layer is safe. In contrast, for an organic circuit board, the openings are formed on a solder mask that is normally composed of a photoimagable polymer. However, any person skilled in the organic circuit board art would know that photoimagable polymers are very sensitive, and that plasma etching will damage the solder mask.

Second, Fig. 2.4 on page 18 of this publication discloses a solder electroplating process where step d removes the photo resister and etches the UBM (under bump metallurgy) which is composed of Ti/Cu/Au (see page 13 of the publication). The UBM is formed on the passivation layer, and both the UBM and the passivation layer are stable materials. Thus, in a conventional UBM process, the photo resister stripper uses a strong base to dissolve the photo resister, and uses a strong acid to etch the UBM. In contrast, for organic circuit boards, since the solder mask is a very sensitive material, any person skilled in the organic circuit board art would know that using a strong base and a strong acid to strip the photo resister and to etch the seed layer will attack the solder mask. In organic circuit board processing, aqueous alkaline solution is normally used to swell, and then strip, the photo resister, and NH4OH or NH4Cl is normally used to etch the seed layer.

In light of the above, Higdon's reference to a "flexible circuit" in column 1, lines 23-25 must be viewed in the context in which it was raised: a discussion of the prior art and its drawbacks. In addition, the fact that ceramic was mentioned in this language would further teach away from organic substrates because ceramic substrates and IC chips share the same properties. For these reasons, a person skilled in the organic circuit board art will not interpret this passing reference to a

"flexible circuit" as meaning that the steps disclosed in Higdon can be applied to an organic circuit board. In fact, this person would know that Higdon's steps would damage an organic circuit board.

The Examiner's reliance of column 1, lines 23-25 of Higdon is based on improper hindsight reconstruction. "It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a 'blueprint.' When prior art references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself." Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985). Furthermore, "a rejection cannot be predicated on the mere identification [in a prior art reference] of claimed limitations. Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kotzab, 208 F.3d 1352, 54 USPQ2d 1308 (Fed. Cir. 2000).

Thus, a person skilled in the art would readily recognize that the techniques and processes used for IC chips cannot be applied to organic circuit boards. For this reason, claim 24 is distinguishable from Higdon, and claim 24 (and claims 25-33 and 44-45 depending therefrom) are in condition for allowance.

In addition, the most common method for formation of pre-solder bumps on the circuit board is the stencil printing method. According to practical experiences, stencil printing will become infeasible once the bump pitch is decreased below ~0.15 millimeters. In contrast, the solder bumps deposited by electroplating offers the ability to further reduce bump pitch down to below 0.15 millimeters. The present invention discloses an electroplating process for fabricating solder bumps on the contact pads of the organic circuit board, which offers good plating and fine bump pitch, wherein the solder bumps are used to produce electroplated solders to contact the electroplated pad or metal bump of the IC chip for forming flip chip joints between the IC chip and an organic circuit board. However, column 1 of Higdon does not disclose electroplating "bumps" on an organic circuit board, as recited in claim 24. Thus, it is respectfully submitted that this limitation is also not met by Higdon.

B. Claims 44-45 are patentably distinguished over Higdon within the meaning of 35 U.S.C. §102(e) and 35 U.S.C. §103(a).

In the Final Office Action dated December 29, 2004, claim 44 was rejected under 35 U.S.C. 102(e) as being anticipated by Higdon, and claim 45 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Higdon in view of Bhatt. As shown below, these rejections are improper and should be reversed and withdrawn.

Claims 44-45 are submitted to define additional patentable subject matter.

First, ***claim 44*** depends from claim 24 and recites that the organic circuit board includes insulative layers made of an organic material. Higdon does not disclose that its substrate includes insulative layers made of an organic material. Thus, claim 44 is submitted to be allowable for the same reasons as claim 24.

Second, ***claim 45*** depends from claim 44 and recites that the organic material is selected from the group consisting of epoxy resin, polyimide, bismeleimide triazine, cyanate ester, polybenzocyclobutene, and a glass fiber composite. These materials are the materials that would be used in an organic circuit board, and are clearly not disclosed in Higdon. Given the nature of the teachings in Higdon (as described above), any attempt to add the teachings of another reference (e.g., Bhatt) would be based on impermissible hindsight reconstruction.

Thus, for the reasons set forth above, the Examiner has failed to make a *prima facie* case of obviousness against claim 45. "To establish a *prima facie* case of obviousness, [the accused infringer] must show 'some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Tec Air, Inc. v. Denso Manufacturing Michigan Inc., 192 F.3d 1353, 52 USPQ2d 1294 (Fed. Cir. 1999). It is well settled patent law that "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." Carella v. Starlight Archery, 804 F.2d 1091, 231 USPQ 644 (Fed. Cir. 1986). "To prevent the use of hindsight based on the invention to defeat patentability of the invention, [the Federal Circuit] requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons the skilled artison, confronted with the same problems as the inventor

and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998).

Even when all of the elements of the combination are within a single prior art reference, the principle still requires motivation or suggestion to modify a disclosed embodiment in the prior art reference. For example, the court in In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), found that the Examiner's suggested modification of a structure disclosed in a single prior art reference would not have been obvious, because no motivation to make the modification was shown and because the modification would have destroyed the intended operation of the prior art device. "The fact that a prior art device could be modified so as to produce the claimed device is not a basis for an obviousness rejection unless the prior art suggested the desirability of such a modification. Id., See also In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); and In re Mills 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Applying the reasoning of the Federal Circuit to the present obviousness rejection of claim 45, the question is whether it would have been obvious from a fair reading of Higdon and Bhatt to modify the steps disclosed in Higdon by using the materials recited in claim 45. The only alleged motivation or desirability suggested by the Examiner for making the combination is that this would be well-known in semiconductor manufacture. However, as noted above, the use of Higdon's steps with such materials would damage the organic circuit board. Thus, the alleged motivation suggested by the Examiner is improper. The Examiner has, thus, failed to make a *prima facie* case of obviousness.as to claim 45 under the provisions of 35 U.S.C. 103(a). The rejection of claim 45 should, therefore, be reversed and withdrawn.

9. CONCLUSION

In view of the foregoing, Appellant respectfully submits that claims 24-33 and 44-45 are patentable over the prior art and that the rejections as stated in the final Office Action of December 29, 2004, should be reversed and withdrawn.

Respectfully submitted,

Date: May 25, 2005

Raymond Sun, 35,699
Attorney for Applicant

CERTIFICATE OF MAILING

I hereby certify that this paper and its enclosures are being deposited with the United States Postal service as First Class Mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner of Patents, PO Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Date: May 25, 2005 By: _____
Raymond Sun

CLAIMS ON APPEAL - 37 C.F.R. § 1.192(c)(9)

1-23. (Canceled).

24. (ORIGINAL) A method of forming electroplated solder on an organic circuit board for making flip chip joints and board to board solder joints, comprising:
providing an organic circuit board including a surface bearing electrical circuitry that includes at least a contact pad;
forming a solder mask layer on said surface, said solder mask being patterned to expose said contact pad;
forming a thin metal seed layer over said surface, said seed layer being solely made of a first metal material;
forming a resist layer with at least one opening located at said contact pad that is deposited over said seed layer;
forming a solder bump in said opening by electroplating, said solder bump containing at least said first metal material; and
removing said resist layer and said seed layer beneath said resist layer;
wherein said seed layer beneath said solder bump dissolves completely into said solder bump after a reflow process, and disappears.

25. (ORIGINAL) The method of claim 24, wherein said first metal material is selected from a group consisting of copper and tin.

26. (ORIGINAL) The method of claim 24, wherein said seed layer has a thickness less than 0.005 millimeter.

27. (ORIGINAL) The method of claim 24, wherein said seed layer is made of physical vapor deposition method.

28. (ORIGINAL) The method of claim 24, wherein said seed layer is made of chemical vapor deposition method.

29. (ORIGINAL) The method of claim 24, wherein said seed layer is made of electroless plating method.

30. (ORIGINAL) The method of claim 29, further comprising a step before forming said thin metal seed layer:
coating the surfaces of the solder mask and the contact pad with aqueous solutions which at least contains copper ions and then performing a reduction process of said copper ions to form a thin copper film on said surfaces, wherein there is no reduction of noble metal ions.

31. (ORIGINAL) The method of claim 30, wherein said noble metal is selected from a group consisting of palladium, gold and silver.

32. (ORIGINAL) The method of claim 24, further comprising a step before forming said thin metal seed layer:
forming a barrier layer on said contact pad.

33. (ORIGINAL) The method of claim 32, wherein said barrier layer is made of metals selected from a group consisting of copper, tin, nickel, chromium, titanium, copper-chromium alloy, tin-lead alloy, and alloys thereof.

34-43 (Canceled).

44. (NEW) The method of claim 24, wherein said organic circuit board includes insulative layers made of an organic material.

45. (NEW) The method of claim 44, wherein said organic material is selected from the group consisting of epoxy resin, polyimide, bismeleimide triazine, cyanate ester, polybenzocyclobutene, and a glass fiber composite.

UBM Formation on Single Die/Dice for Flip Chip Applications

By

Suwanna Jittinorasett

Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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Solder bump, Single die

UBM Formation on Single Die/Dice for Flip Chip Applications

by

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Electrical Engineering

Abstract

This thesis presents the low cost process for UBM formation on aluminum pads of single die/dice for Flip Chip applications. The UBM (Under Bump Metallization) is required in solder bump structure to provide adhesion/diffusion barrier layer, solder wettable layer, and oxidation barrier layer between the bonding pads of the die and the bumps. Typically, UBM is deposited on the whole wafers by sputtering, evaporation, or electroless plating. These deposition techniques are not practical for UBM formation on single die/dice, thus preventing Flip Chip technology to be applied in applications where the whole wafers are not available. The process presented in this thesis has been developed to overcome this problem. The developed UBM formation process allows the UBM layer to be deposited on a single die, thus eliminating the requirement to have the whole wafer in the deposition process. With the combination of the UBM formation process developed in this work and a suitable bump formation technique, solder bumping on a single die can be achieved, thus making Flip Chip technology available for use in low volume applications and prototyping stages.

The developed UBM formation process consists of two major steps; temporary die attach process and UBM deposition process. The first process is developed using thermoplastic adhesive film. The second process is developed using electroless nickel plating, followed by gold immersion. It has been demonstrated in this thesis that the developed process can be used to form the UBM layer on the die successfully regardless of the die size and the complexity of the die pattern, and that this process does not damage nor affect electrically the sensitive die.

2.3 Solder Bump Structure for Flip Chip Interconnect

Solder bump structure consists of the following,

- Under bump metallurgy (UBM)
- Solder bump

Figure 2.1 shows the solder bump structure.

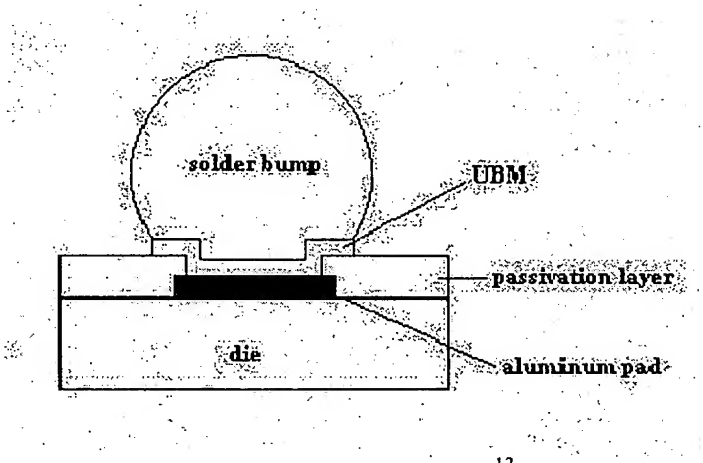

Figure 2.1 Solder bump structure[13].

2.3.1 Under bump metallurgy (UBM)

Solder cannot bond directly to aluminum. The UBM, the interface metals between aluminum pads and solder bumps, is required to provide adhesion, diffusion barrier, and solder wettable layers. UBM is a necessary structure to achieve reliable solder bump interconnects.

2.3.1.1 Requirements of UBM

UBM should have or provide the following capabilities [8],

- Good adhesion to bonding pad metallization and wafer passivation

  UBM must adhere well to both the bonding pad metallization and the passivation layer of wafers. Aluminum is common IC metallization. Typical passivation materials are nitride, oxide, and polyimide. It is important that the passivation layer is pin hole free since pin holes can cause damages to the IC circuit underneath during UBM

deposition process.

- Good ohmic contact to bonding pad metallization

  To achieve good ohmic contact, aluminum oxide on bonding pad surface has to be removed by back sputtering or chemical etching before UBM deposition.

- Solder diffusion barrier

  UBM must provide a diffusion barrier between the solder and the bonding pad Metallization.

- Solder wettable surface

  The final layer of UBM structure must be solder wettable. This is the layer that bond to the solder bump.

- Oxidation barrier

  To assure good solderibility, UBM must not oxidize during solder bump formation process.

- Minimum stress on silicon

  UBM structure must not cause excessive stress on the silicon underneath it. The excessive stress can cause the fracture and cratering of underlying silicon. Cratering of silicon is considered to be a reliability defect.

2.3.1.2 UBM structure

UBM are multilayer thin films. Typically, UBM consists of three layers [4,9,10,11,12].

- Adhesion and diffusion barrier layer.

  Function: Form strong bond with bonding pad metallization and IC passivation layer and prevent diffusion between bonding pad metallization and solder bumps.

  Typical metals used: Chromium (Cr), titanium (Ti), titanium/tungsten (Ti/W), nickel (Ni), palladium (Pd), and Molybdenum (Mo).

  Typical thickness: ~0.15-0.2 μm.

- Solder wettable layer

  Function: provide surface for solder bump to adhere to.

  Typical metals used: Copper (Cu), nickel (Ni) and palladium (Pd).

  Typical thickness: ~1-5 μm.

• Oxidation barrier layer

Function: prevent UBM structure from oxidation.

Typical metals used: Gold (Au).

Typical thickness: ~0.05-0.1 μm.

There are many possible combinations of thin film layers for UBM such as Ti/Cu/Au, Ti/Cu, Ti/Cu/Ni, TiW/Cu/Au, Cr/Cu/Au, Ni/Au, Ti/Ni/Pd, and Mo/Pd. However, the structure of UBM affects greatly the reliability of UBM itself. For example, it has been reported that Ti/Cu/Ni (electroless Ni) UBM has better adhesion strength than Ti/Cu UBM [12]. UBM structure also has effects on reliability of connections between UBM and bonding pad and between the UBM and the solder bumps. To achieve reliable connection between UBM and solder bumps, UBM must be compatible with the solder alloys used for solder bump. UBM suitable for high lead solders may not work well with high tin solders (eutectic solders). For example, Cu is a good solder wettable layer for high lead solder with 3-5% of tin, but it is not suitable for high tin solder since Sn react rapidly with Cu and form Sn-Cu intermetallic compound. If Cu is completely consumed, solder will dewet from the bond pads [8,9,10].

2.3.1.3 UBM deposition techniques

UBM can be deposited by sputtering, evaporation or electroless plating [5].

• *Sputtering:*

In this technique, thin film layers sequentially sputtered on the entire wafer. Next, photolithography process is performed to pattern the UBM. All UBM will be etched away except over the boding pads.

• *Evaporation:*

Thin film layers are successively evaporated on the entire wafer and patterned using photolithography process. The other method is evaporation with the use of a mask. In this method, the metal mask or photoresist is used to cover the entire wafer except the bond pads and UBM is selectively deposited on the opening area of the mask. The later method is suitable when solder bumps are formed by evaporation since both UBM and solder bumps can be formed using the same mask.

• *Electroless plating:*

Normally, electroless plating is used to deposit nickel UBM. Electroless nickel plating is a wet chemical and maskless process. Nickel is selectivelly formed on the aluminum pads. However, aluminum surface must be prepared before plating. Zincation is the common used process to pretreate aluminum. Electroless plating is a low cost process since it requires fewer processing steps and no patterning or vacuum facility is necessary. Electroless nickel plating process will be discussed in detail in a later topic.

2.3.2 Solder bump

The most common use solder for solder bump is lead/tin(Pb/Sn) alloy since it offers the fully reflowable solder bumps. The fully reflowable solder bump have the capability of self-alignment and collapse during reflow. Self alignment reduces the required accuracy for the process of placing the bare chips onto the substrate. Hence, no special placement machine is required. The collapse property reduces the non-planarity problem [8]. High Pb solders such as 95Pb/5Sn or 97Pb/3Sn have high reflow temperature (~330-350 °C). For applications that require low operating temperature such as flip chip on organic substrates, high Sn solders will be used. High Sn solders such as eutectic solder (37Pb/63Sn) have reflow temperature at ~200 °C [10]. However, since lead is toxic, lead-free solder alloy needs to be developed.

2.3.2.1 Solder bumping techniques

• ***Evaporation***

In evaporation process, a metal mask is used to pattern both UBM and solder bump deposition. First, UBM thin films are sequentially evaporated and deposited on the bond pads through the openings of the metal mask. Next, solder is evaporated and the bumps are formed on the bond pads. The deposited bumps have cone shape with the height about 100-125 μm. The bump height depends on the volume of evaporated solder which is a function of the distance between the metal mask and the wafer and the mask opening size. Since lead has higher vapor pressure than tin, lead deposits first, followed by tin. This results in the bump with Pb rich solder at the bottom and Sn rich solder on the top [5,13]. After the evaporation process is achieved, solder is reflowed to homogenize Pb-Sn

layer and to form the ball-shape bump. Figure 2.2 shows the process flow of solder evaporation using metal mask to pattern the UBM and the bumps. An alternative to evaporation using metal mask is lift-off process [4,14]. In lift-off process, photoresist is used instead of metal mask. Thick layer of photoresist is spin coated and patterned with opening on the bond pad area. Then, solder is evaporated and deposited on the bond pads and on the top of photoresist. The deposited solder on the bond pads and on the photoresist is not connected. Next, photoresist is stripped which will also lift off the deposited solder on the top.

• ***Printing***

First UBM is deposited and patterned. Then, solder paste is printed in the same way as conventional printing for thick film materials [5,13]. Both stencil and screen can be used. The volume and the height of the printed paste are determined by the opening size and the thickness of the stencil. Since the opening size of stencil is limited by the pad pitch, the stencil should be as thick as possible to increase the volume of printed paste. However, the higher thickness increases the wetted area of the stencil, thus increasing the chance that the solder will clog the stencil. Hence, it is important to select the proper stencil geometry[15]. After printing, the printed solder is reflowed to form the ball bumps and flux residues are cleaned. Figure 2.3 shows solder printing process flow.

• ***Electroplating***

In electroplating process [5,16,17], UBM is used as a seed layer for plating. First, UBM is deposited on the entire wafer. Then, thick photoresist is coated and patterned such that there are openings on the bond pad area. The photoresist determines the shape and the height of the plated bumps. Before electroplating, the photoresist residues on the openings are removed by plasma etching. The photoresist residues can reduce the adhesion of the bumps, increase contact resistance, and cause an inhomogeneous growth of the electroplated layers [18]. Next, the wafer is electroplated in a plating solution with the current applied and the wafer as the cathode. The plated solder has a mushroom shape. For electroplating, compared to other deposition processes, it is difficult to control the composition and the height of the plated bump [19]. After plating, photoresist is stripped. UBM is removed by wet etching using plated solder as etching resist, then,

solder is reflowed into ball shape. The other method is to reflow the plated bump first, and etch the UBM later. Figure 2.4 shows the process flow of electroplating.

• ***Stud or ball bumping***

Stud bumping uses the standard wirebonding process to form the bumps. Both gold wire and Pb based wire can be used. The process of stud bumping is the same as that of wire bonding. The only difference is that after the ball is formed at the tip of the wire and bonded to the bond pad, the wire is broken just above the ball as shown in Figure 2.5. UBM compatible with the wire used is required. After bumping, the bump can be reflowed into sphere or coined to get the flat surface with uniform bump height. Typically, stud bump is used with conductive adhesive (both isotropic and anisotropic conductive adhesive) or additional solder [5,20].

• ***Ball placement***

In this method, preformed solder balls are used to form the bumps. First, flux is applied on the bond pads. Then, solder balls are placed using special techniques and machines [21,22,23] and held in place on the pads by the tackiness of flux. Next, the balls are reflowed and bonded to UBM on the pads.

• ***Solder transfer***

In this process, solder bumps are formed on carriers, and then transferred to the bond pads [14,24]. Carriers must be the materials that are nonwettable with solder such as silicon wafer, heat-resistant glass sheet. First, the bumps are formed on the carrier using evaporation process. The bumps are formed such that the patterns of the bumps are exactly the same as those of the chip pads. Both metal mask and lift-off process can be used to pattern the carrier. A thin layer of gold about 1000 A° thick may be deposited prior to bump deposition. This gold layer is used to promote the adhesion between the solder and the carrier, thus help prevent separation of the solder from the carrier during processing and increase the time period before the solder is molten and separate from the carrier so that it has enough time to wet to the UBM on the chip pads. The next step is the transfer process. If the bumps are transferred to the wafer, the carrier will be singulated and placed on fluxed wafer. If the bumps are transferred to the individual die, the die will be placed on fluxed carrier. Then, the reflow process is performed and the bumps are dewetted from the carrier and bonded to the target pads. The carrier still sticks

to the bumps due to flux residue. Finally, the flux residues are cleaned and the carrier is separated. Figure 2.6 shows the solder transfer process flow.

Among these bumping techniques, the first three techniques can be used to form the bumps on wafer only, whereas the remaining techniques can be used for both the wafer and the single chip bumping.

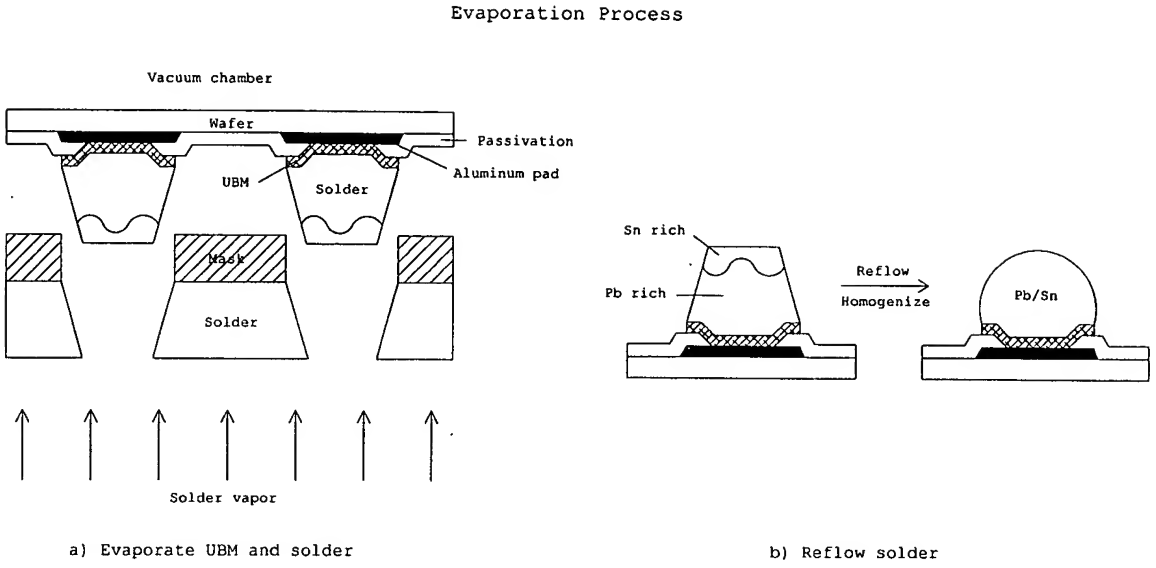

Figure 2.2 Solder evaporation process[5,13].

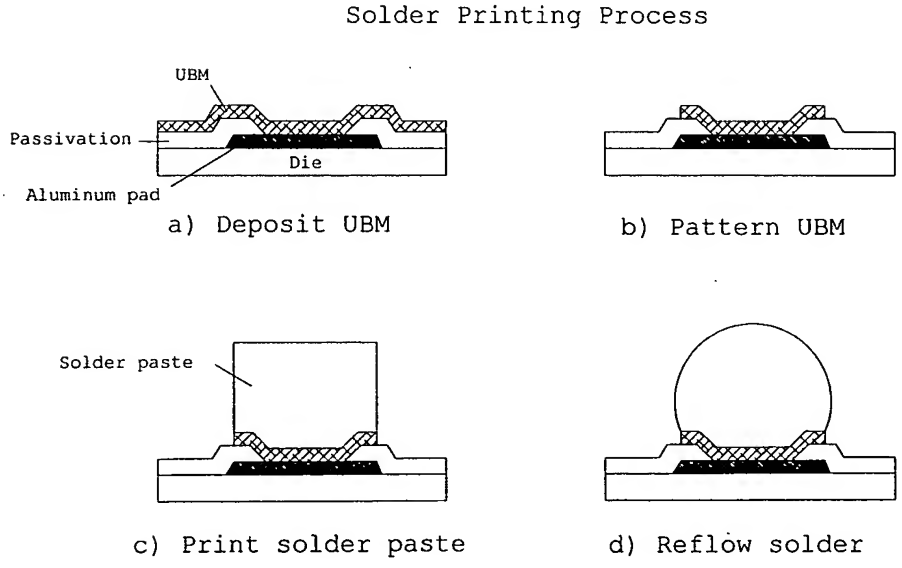

Figure 2.3 Solder printing process[5].

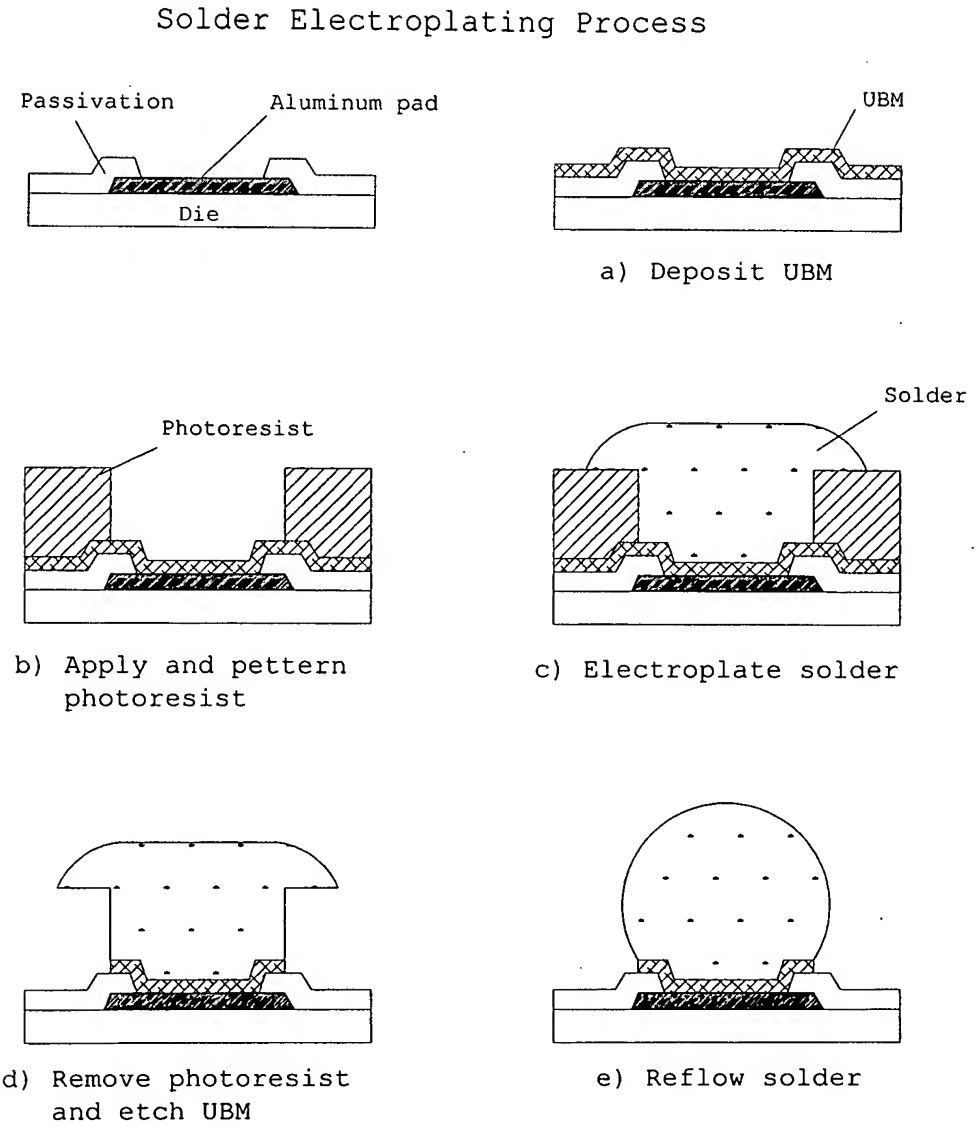

Figure 2.4 Solder electroplating process[5].

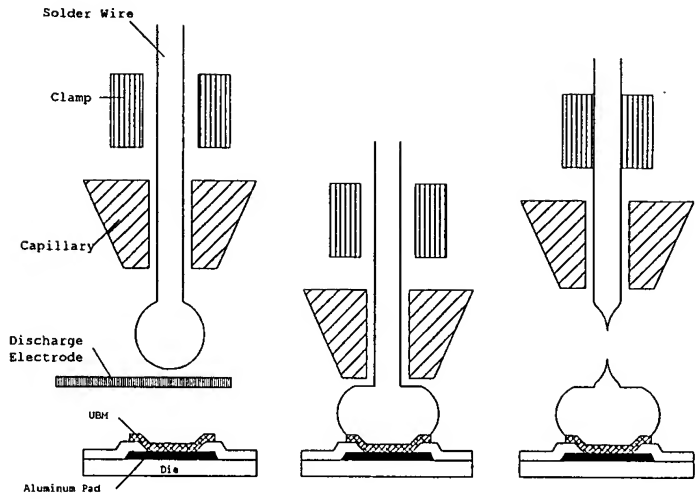

Figure 2.5 Stud bumping[13].

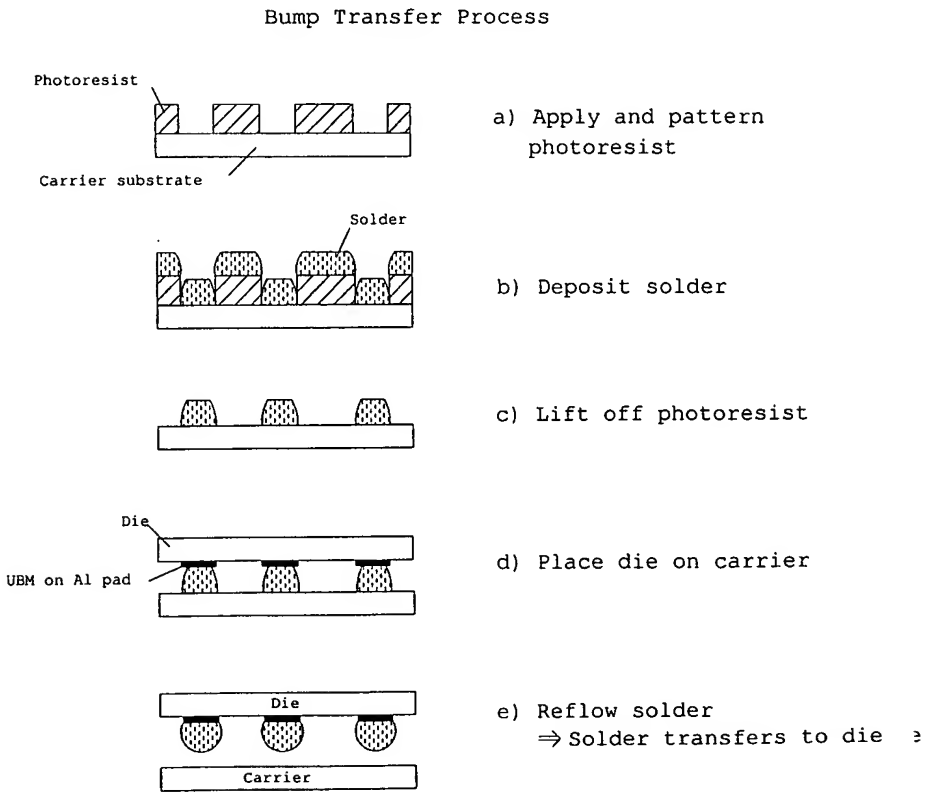

Figure 2.6 Solder transfer process[14].